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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/763,554	01/23/2004	Hirokazu Honda	NEC 26485	7561

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HAYES SOLOWAY P.C.
3450 E. SUNRISE DRIVE, SUITE 140
TUCSON, AZ 85718

EXAMINER	
WILLIAMS, ALEXANDER O	
ART UNIT	PAPER NUMBER
2826	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/763,554	HONDA, HIROKAZU	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 October 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-9,16,17 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-9,16,17 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Serial Number: 10/763554 Attorney's Docket #: NEC 26485
Filing Date: 1/23/2004; priority to 2/3/2003 and 12/10/2003

Applicant: Honda

Examiner: Alexander Williams

Applicant's Amendment filed 10/20/08 to the election of the species I, figures 1a, 1b, 8a-8h and 12a (claims 1-9, 16-18 and 19), filed 9/26/05, has been acknowledged.

This application contains claims 10-15, 18 and 19 drawn to an invention non-elected without traverse.

Claims 2 and 3 have been cancelled.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4-9, 16, 17 and 20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Baba Mikio (Japan Patent Publication # 2001-244362 A) in view of Ryoichi (Japan Patent Publication # 6-61383) and further in view of Kajiwara et al. (U.S. Patent Application Publication # 2002/0056906 A1).

1. Baba Mikio (figures 1 to 4) specifically figure 1 show a semiconductor device comprising: a semiconductor chip **2** mounted on a mounting substrate **1**; a first resin **6** filling a gap between the semiconductor chip and the mounting substrate; a stiffener **5** surrounding the semiconductor chip, the stiffener being adhered

to the mounting substrate with a first adhesive **4**; and a second resin **7** partially filling a space between the semiconductor chip and the stiffener in contact with the first resin, the first resin being different in a thermal expansion coefficient from the second resin. Mikio fail to explicitly show a second resin filling a space between the semiconductor chip and the stiffener in contact with the first resin, wherein the first and second resin comprises an epoxy resin main component and an inorganic filler component and wherein the epoxy resin main component is the same in the first resin and the second resin and the inorganic filler component f the first resin is different than the inorganic filler component of the second resin.

Ochiai Ryoichi is cited for showing a semiconductor device. Specifically, Ryoichi (figures 1 to 3) specifically figure 2 discloses a semiconductor device comprising: a semiconductor chip **2** mounted on a mounting substrate **1**; a first resin **21** filling a gap between the semiconductor chip and the mounting substrate; a stiffener **1** surrounding the semiconductor chip, the stiffener being adhered to the mounting substrate with a first adhesive; and a second resin **22** filling a space between the semiconductor chip and the stiffener in contact with the first resin, the first resin being different **(being different is interpret to means not the other)** in a thermal expansion coefficient from the second resin for the purpose of enhancing a flip chip device in heat dissipating properties and an inter-pad connection between the flip device and a ceramic package in reliability.

Kajiwara et al. is cited for showing a flip chip assembly structure for semiconductor device. Specifically, Kajiwara et al. (figures 1 to 32) specifically figure 22 discloses the first

and second resin comprises an epoxy resin main component and an inorganic filler component and wherein the epoxy resin main component is the same in the first resin and the second resin and the inorganic filler component **7** of the first resin is different than the inorganic filler component **221** of the second resin for the purpose of reducing the problem of reducing drawing the moisture to expand under the environment of the high temperature and the high humidity, allowing the resistance to increase.

Summary of Invention Paragraph - BSTX (16):

[0014] In addition, the metallic electrodes of the semiconductor chip and the internal connection terminals of the printed circuit board are electrically connected to each other through the precious metal bumps by the metal joining; the melting point of a metal material of which each of the connection parts is made is equal to or higher than 275 degrees; the resin (under fill) containing 50 vol % or more inorganic fillers is led into the space defined between the chip and the board; resin is formed in such a way as to become void-free; and the fluctuation, of the containing rate of inorganic fillers contained in resin, which is dependent of the places is made equal to or lower than 10% or less (with respect to the definition of the fluctuation, the fluctuation of the filler containing rate is obtained by cutting out resin of 1 millimeters square from an arbitrary place within the chip surface, and the value which is obtained by dividing the difference between the maximum value and the minimum value thus obtained from that fluctuation by the mean containing rate is expressed in the form of the fluctuation rate).

Detail Description Paragraph - DETX (35):

[0086] In this connection, while not particularly illustrated, when subjecting the semiconductor assembly product in which the filler containing rate in the resin sheet is 50% and the plane distribution of the fillers is equal to or lower than .+-.5% or less at a maximum with the dispersion in the filler containing rate in 1 mm square and the semiconductor assembly product in which the liquid resin having the same containing rate is filled after completion of the flip chip

joining and which is free from the voids to the same temperature cycling test in order to carry out the comparison, it is confirmed that there is the clear difference in the number of times of temperature cycles up to which the product is brought to the disconnection failure, and the product which is manufactured by supplying the resin in a sheet-like shape has the longer life. As this cause, it becomes clear as the result of the analysis that the filler distribution between the chip and the board in the resin sheet supplying system roughly follows the filler distribution in the resin sheet state, whereas in the liquid resin supplying system, there occurs the phenomenon that a lot of fillers are present in the upstream side area of the supply and there are not many fillers in the downstream side area, and hence the difference of 20% at a maximum occurs in the above-mentioned semiconductor assembly products.

Detail Description Paragraph - DETX (40):

[0091] FIG. 11 shows the Weibull plot of the failure occurrence rate when the samples having the different filler containing amounts are subjected to the temperature cycling test. Since the under fill resin has the high thermal expansion coefficient, it is short-lived in the state in which there is no filler. When the filler material which has the lower thermal expansion coefficient than that of the under fill resin gets mixed therewith to decrease the thermal expansion, the life is lengthened. In this case, when employing the under fill resin having the filler containing rate of 50% or the two-layers under fill, there is shown the life exceeding 1,000 cycles. The method wherein the under fill having the filler containing rate of 70% or more can be filled in a void free manner is only the method according to the present invention. Thus, it is said that the two-layers system is not the possible structure until the method of the present invention has been made. That is, it is possible to provide the highly reliable flip chip assembly products by the embodiment of the present invention.

Detail Description Paragraph - DETX (139):

[0190] (15) A method of loading a semiconductor chip on a printed circuit board in a face down manner, a flip chip assembly method comprising: the process of forming precious metal bumps on electrodes of said semiconductor chip; the process of placing a plurality sheets of semi-cured resin sheets

having different containing rates of inorganic fillers on a predetermined position on said printed circuit board to load thereon said semiconductor chip with said precious metal bumps aligned with internal connection terminals of said printed circuit board; and the process of after having applied from the rear face side of said semiconductor chip, the heat, the load and the ultrasonic wave by a joining tool to push said precious metal bumps into said resin sheet and processing said precious metal bumps thereagainst to join compressively said precious metal bumps to a precious metal film formed on said internal connection terminals, carrying out the heating processing to cure said resin sheet.

4. The semiconductor device as claimed in claim 1, the combination with Ryoichi show wherein the first resin includes an underfill part filling the gap between the semiconductor chip and the mounting substrate, and a fillet part extended from a region of the semiconductor chip.

5. The semiconductor device as claimed in clam 1, the combination with Mikio show wherein the first adhesive is larger in a thermal expansion coefficient than the second resin.

6. The semiconductor device as claimed in claim 4, the combination with Mikio show wherein the second resin **22** is in contact with inner walls of the stiffener **1**, the fillet part **21**, the mounting substrate **1** and each of side faces of the semiconductor chip **2**.

7. Baba Mikio (figures 1 to 4) specifically figure 1 show a semiconductor device comprising: a semiconductor chip **2** mounted on a mounting substrate **1**; a first resin **6** filling a gap between the semiconductor chip and the mounting substrate; a stiffener **5** surrounding the semiconductor chip, the stiffener being made of a different material from the second resin; a second resin **4** filling a space between the semiconductor chip and the stiffener in contact with the first resin, the first resin being different

in a thermal expansion coefficient from the second resin; and a lid **9** for covering the stiffener and the semiconductor chip, wherein the lid is bonded to the stiffener and a backside of the semiconductor chip with an adhesive. Mikio fail to explicitly show a second resin filling a space between the semiconductor chip and the stiffener in contact with the first resin, wherein the first and second resin comprises an epoxy resin main component and an inorganic filler component and wherein the epoxy resin main component is the same in the first resin and the second resin and the inorganic filler component f the first resin is different than the inorganic filler component of the second resin.

Ochiai Ryoichi is cited for showing a semiconductor device. Specifically, Ryoichi (figures 1 to 3) specifically figure 2 discloses a semiconductor device comprising: a semiconductor chip **2** mounted on a mounting substrate **1**; a first resin **21** filling a gap between the semiconductor chip and the mounting substrate; a stiffener **1** surrounding the semiconductor chip, the stiffener being adhered to the mounting substrate with a first adhesive; and a second resin **22** filling a space between the semiconductor chip and the stiffener in contact with the first resin, the first resin being different **(being different is interpret to means not the other)** in a thermal expansion coefficient from the second resin for the purpose of enhancing a flip chip device in heat dissipating properties and an inter-pad connection between the flip device and a ceramic package in reliability.

Kajiwara et al. is cited for showing a flip chip assembly structure for semiconductor device. Specifically, Kajiwara et al. (figures 1 to 32) specifically figure 22 discloses the first

and second resin comprises an epoxy resin main component and an inorganic filler component and wherein the epoxy resin main component is the same in the first resin and the second resin and the inorganic filler component **7** of the first resin is different than the inorganic filler component **221** of the second resin for the purpose of reducing the problem of reducing drawing the moisture to expand under the environment of the high temperature and the high humidity, allowing the resistance to increase.

8. The semiconductor device as claimed in claim 7, the combination with Mikio show wherein the second resin **22** is in contact with an inner wall of the lid.

9. The semiconductor device as claimed in claim 1, the combination with Mikio show wherein an elastic modulus of the second resin **22** is larger than an elastic modulus of the first resin **21.**

16. The semiconductor device as claimed in claim 1, the combination with Mikio show wherein the stiffener **(outer portion of 5)** is made of a material selected from the group consisting of Cu, SUS, Al, alumina, silicon, aluminum nitride, and resin.

17. The semiconductor device as claimed in claim 1, the combination with Mikio show wherein each of the first resin **21** and the second resin **22** essentially contains a resin selected from a group consisting of **epoxy**, polyolefin, silicon, cyanate ester, polyimide, polynorbornene resins.

20. The semiconductor device as claimed in claim 1, the combination with either reference showing wherein the semiconductor chip is mounted on the mounting substrate through flip chip bonding.

Therefore, it would have been obvious to one of ordinary skill in the art to use Kajiwara et al.'s different than the inorganic filler components and Ryoichi's second resin to modify Mikio's second resin for the purpose of enhancing a flip chip device in heat dissipating properties and an inter-pad connection between the flip device and a ceramic package in reliability.

Response

Applicant's arguments filed 10/20/08 have been fully considered, but are not found to be persuasive view of the new grounds of rejections detailed above.

The insertion of Applicant's additional claimed language, for example, "in claims 1 and 7" cause for further search and consideration to make this action final.

Applicant's amendment necessitated the new grounds of rejection. Accordingly, **THIS ACTION IS MADE FINAL**. See M.P.E.P. э 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. э 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. э 1.136(a) WILL BE CALCULATED FROM THE

MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571) 272 1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AOW
6/19/08

/Alexander O Williams/
Primary Examiner, Art Unit 2826